



FIG. 1

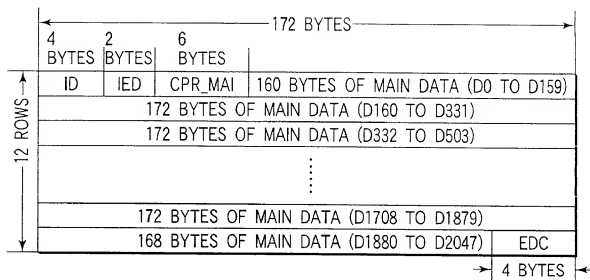


FIG. 2

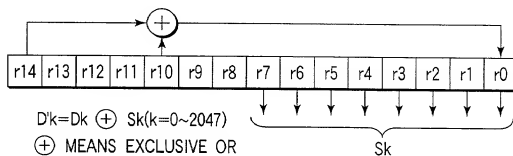


FIG. 3

	172 BYTES						10 BYTES	
16 ROWS	B0,0	B0,1		B0,170	B0,171	B0,172		B0,181
	B1,0	B1,1		B1,170	B1,171	B1,172		B1,181
	B2,0	B2,1		B2,170	B2,171	B2,172		B2,181
	B189,0	B189,1		B189,170	B189,171	B189,172		B189,181
	B190,0	B190,1		B190,170	B190,171	B190,172		B190,181
	B191,0	B191,1		B191,170	B191,171	B191,172		B191,181
	B192,0	B192,1		B192,170	B192,171	B192,172		B192,181
	B207,0	B207,1		B207,170	B207,171	B207,172		B207,181

FIG. 4

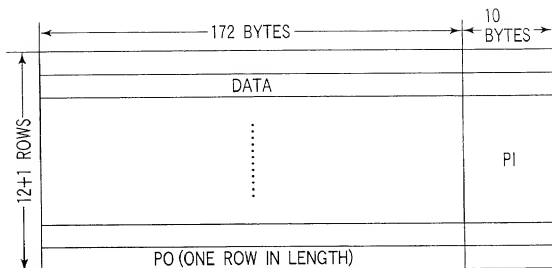


FIG. 5

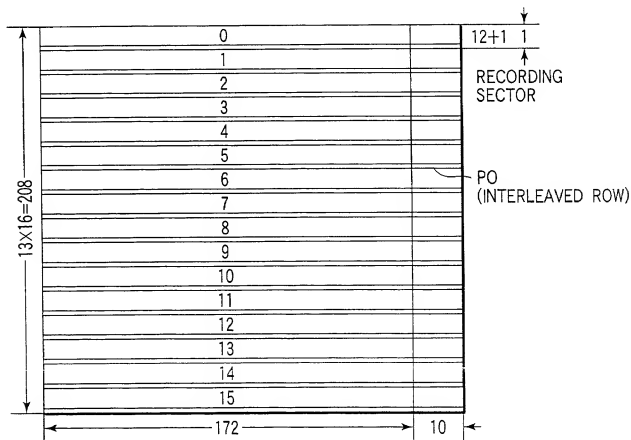


FIG. 6

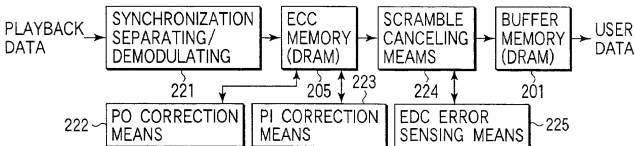
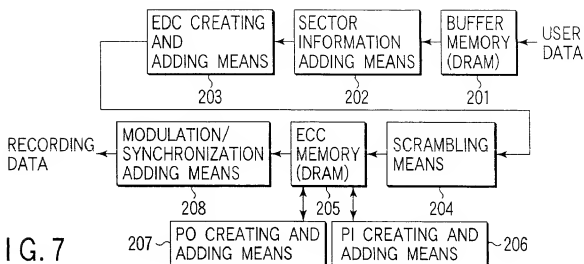
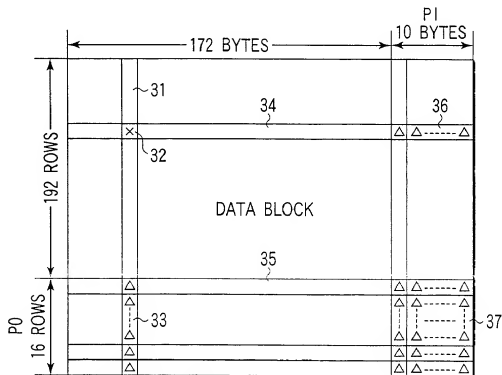


FIG. 8



× MEMORY ERROR
 △ ERROR-CORRECTING CODE CREATED ON THE
 BASIS OF DATA INCLUDING MEMORY ERROR

FIG. 9

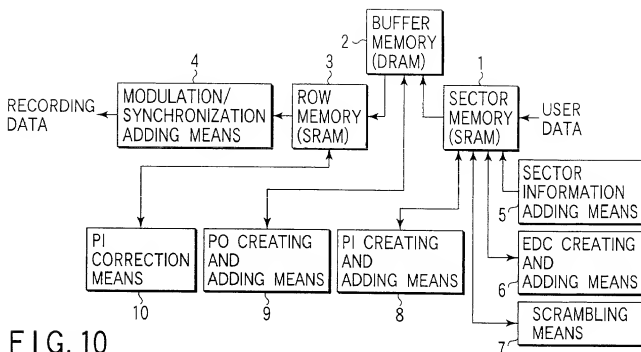


FIG. 10

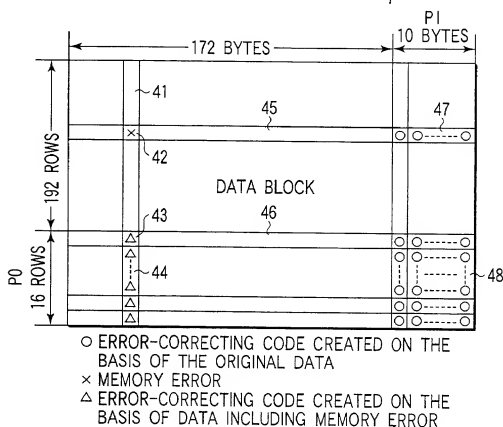


FIG. 11

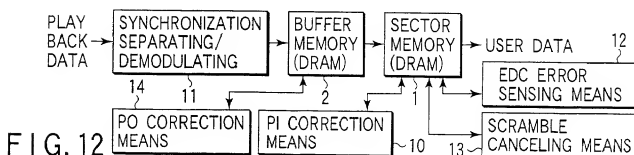


FIG. 12

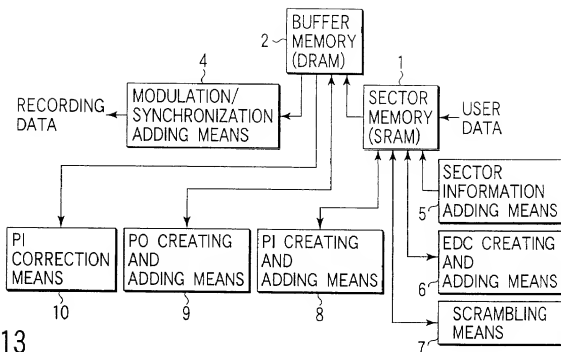


FIG. 13

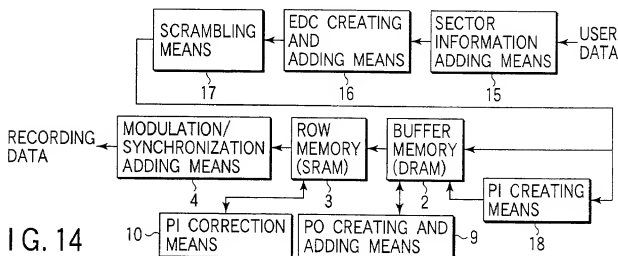


FIG. 14

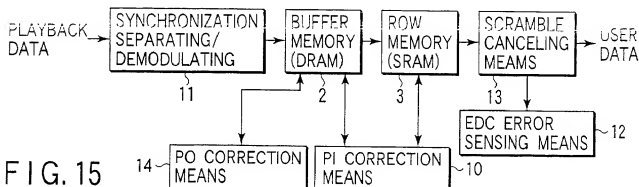
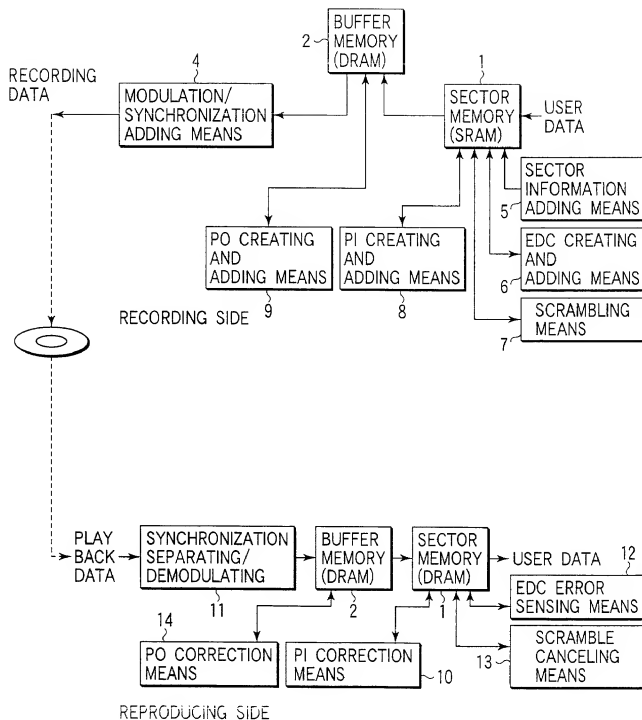


FIG. 15



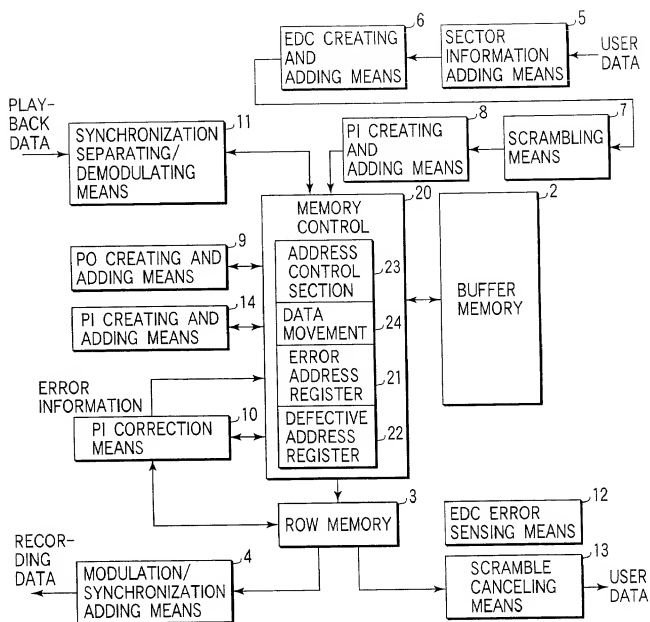


FIG. 17



Diagram illustrating memory layout and error occurrence:

ADDRESS	DATA
A+0	B0, 0
A+1	B0, 1
...	...
A+(J-1)	B0, J-1
A+(J)	X
A+(J+1)	B0, J
A+(J+2)	B0, J+1
...	...
A+182	B0, 181
A+183	B1, 0
A+184	B1, 1
...	...
A+364	B1, 181
A+365	B2, 0
A+366	B2, 1
...	...
A+366x182-1	B207, 180
A+208x182	B207, 181

Annotation: AREA WHERE MEMORY ERROR OCCURS REPEATEDLY (pointing to B0, J)

Annotation: RY (pointing to A+184)

FIG. 18B

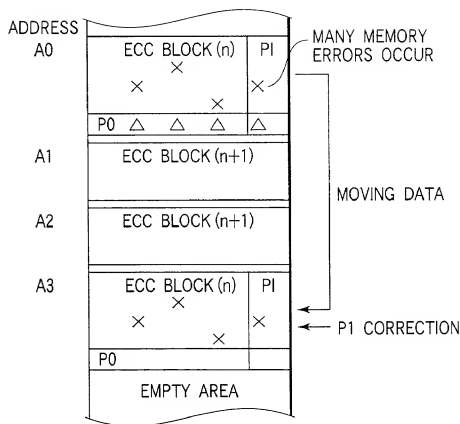


FIG. 19